WEST

Generate Collection | Print

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5526364 A

L12: Entry 1 of 1 File: USPT Jun 11, 1996

US-PAT-NO: 5526364
DOCUMENT-IDENTIFIER: US 5526364 A

TITLE: Apparatus for entering and executing test mode operations for memory

DATE-ISSUED: June 11, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roohparvar; Frankie F.	Cupertino	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Quantum Devices, Inc.	Boise	ID			02

APPL-NO: 8/ 386704
DATE FILED: February 10, 1995

INT-CL: [6] G01 R 31/28

US-CL-ISSUED: 371/22.1; 371/22.3, 371/22.5
US-CL-CURRENT: 714/724; 714/726, 714/733

FIELD-OF-SEARCH: 371/22.1, 371/22.3, 371/22.4, 371/22.5, 371/22.6, 371/24, 371/15.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5077738	December 1991	Larsen et al.	

ART-UNIT: 243
PRIMARY-EXAMINER: Canney; Vincent P.
ATTY-AGENT-FIRM: Merchant Gould Smith Edell Welter & Schmidt

ABSTRACT:

A circuit for generating test-mode signals for memory which uses both hardware and software protection schemes. The circuit enters a test code by receiving a high voltage at two terminals. The high voltage must remain on at least one of the terminals during the test code process. Otherwise, the circuit is reset. The test code contains test code bits and format code bits. The format code bits are the same for all test codes and distinguish the test codes from commands.

41 Claims, 5 Drawing figures

WEST

End of Result Set

Generate Collection Print

L12: Entry 1 of 1 File: USPT Jun 11, 1996

US-PAT-NO: 5526364
DOCUMENT-IDENTIFIER: US 5526364 A

TITLE: Apparatus for entering and executing test mode operations for memory

DATE-ISSUED: June 11, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Roohparvar; Frankie F.	Cupertino	CA		

US-CL-CURRENT: 714/724; 714/726, 714/733

CLAIMS:

What is claimed is:

1. A circuit for generating an enable signal for testing a circuit, comprising:

a first voltage detector for detecting a test-activation voltage;

a second voltage detector for detecting the test-activation voltage;

a first latch for receiving a test signal; and

an enable circuit, coupled to the first and second voltage detectors and the latch. for decoding the test signal to determine if the test signal is valid and for generating an enable signal if the test signal is valid and the first and second voltage detectors detect the test-activation voltage.

2. The circuit of claim 1 wherein the enable circuit generates the enable signal if both the first and second voltage detectors detect a high voltage and either the first or second voltage detector subsequently detects a low voltage.

3. The circuit of claim 1 wherein the enable circuit is enabled upon receiving a voltage above a first predetermined value and the enable circuit is reset if the voltage decreases below a second predetermined value.

4. The circuit of claim 1 wherein the enable circuit decodes the test signal by comparing the test signal with a predetermined value in order to determine if the test signal and the predetermined value match.

5. The circuit of claim 1 wherein the enable circuit resets the enable signal if the test-activation voltage does not remain at the first voltage detector.

6. The circuit of claim 5, further comprising a detector circuit for detecting if the test-activation voltage does not remain at the voltage detector.

7. The circuit of claim 6, wherein the detector circuit comprises:

a second latch coupled to the output of the first voltage detector and to the enable circuit, the second latch maintaining power to the first voltage detector; and

a circuit coupled to the second latch for resetting the second latch.

8. The circuit of claim 1 wherein the test signal comprises format bits and test code bits.

9. The circuit of claim 1 wherein the enable circuit generates the enable signal for testing a flash EPROM.

10. The circuit of claim 1 wherein the enable circuit generates the enable signal for testing an SRAM.

11. The circuit of claim 1 wherein the enable circuit generates the enable signal for testing an EEPROM.

12. The circuit of claim 1 wherein the enable circuit generates the enable signal for testing a DRAM.

13. The circuit of claim 1 wherein the enable circuit is connected to an input to the first latch.

14. The circuit of claim 1 wherein the enable circuit is connected to an output of the first latch.

15. The circuit of claim 1 wherein the circuit is contained within an integrated circuit package.

16. A method for generating an enable signal for testing a circuit, comprising the steps of:

detecting an activation voltage by detecting a high voltage with a first voltage detector and a second voltage detector and subsequently detecting a low voltage with the first voltage detector or the second voltage detector;

receiving a test signal;

decoding the test signal to determine if the test signal is valid; and

generating an enable signal when the activation voltage is detected if the test signal is valid, and when the high voltage is detected with both the first and second voltage detectors and when the low voltage is subsequently detected with either the first or second voltage detector.

17. The method of claim 16 wherein:

the detecting step comprises the steps of detecting a high voltage with both a first voltage detector and a second voltage detector and subsequently detecting a low voltage with either the first or second voltage detector; and

the generating step comprises the step of generating the enable signal when the high voltage is detected with both the first and second voltage detectors and the low voltage is subsequently detected with either the first or second voltage detector.

18. The method of claim 16 wherein the generating step generates the enable signal upon receiving a voltage above a first predetermined value and resets the enable signal if the voltage decreases below a second predetermined value.

19. The methodof claim 16 wherein the decoding step further comprises the step of comparing the test signal with a predetermined value to determine if the test signal and the predetermined value match.

20. The method of claim 16 wherein the generating step further comprises the step of resetting the enable signal if the test-activation voltage is not continuously detected during the decoding step.

21. The method of claim 16 wherein the detecting step further comprises the steps of:

setting a latch upon detecting the test-activation voltage, the setting of the latch maintaining power to a voltage detector for detecting the activation voltage; and

resetting the latch if the test-activation voltage decreases to a value less than a

predetermined value.

22. The method of claim 16 wherein the generating step generates the enable signal for testing a flash EPROM.

23. The circuit of claim 16 wherein the generating step generates the enable signal for testing an SRAM.

24. The circuit of claim 16 wherein the generating step generates the enable signal for testing an EEPROM.

25. The circuit of claim 16 wherein the generating step generates the enable signal for testing a DRAM.

26. A computer with a circuit for generating an enable signal for testing a circuit, comprising:

a processor;

a clock circuit connected to the processor;

a module, connected to the processor, for interfacing the processor with peripheral devices; and

a memory module connected to the processor, comprising: a circuit for generating an enable signal for testing the memory module, comprising:

a first voltage detector for detecting a test-activation voltage;

a second voltage detector for detecting the test-activation voltage;

a first latch for receiving a test signal; and

an enable circuit, coupled to the first and second voltage detectors and the latch, for decoding the test signal to determine if the test signal is valid and for generating an enable signal if the test signal is valid and the first and second voltage detectors detect the test-activation voltage.

27. The computer of claim 26 wherein the enable circuit generates the enable signal if both the first and second voltage detectors detect a high voltage and either the first or second voltage detector subsequently detects a low voltage.

28. The computer of claim 26 wherein the enable circuit is enabled upon receiving a voltage above a first predetermined value and the enable circuit is reset if the voltage decreases below a second predetermined value.

29. The computer of claim 26 wherein the enable circuit decodes the test signal by comparing the test signal with a predetermined value in order to determine if the test signal and the predetermined value match.

30. The computer of claim 26 wherein the enable circuit resets the enable signal if the test-activation voltage does not remain at the first voltage detector.

31. The computer of claim 30, further comprising a detector circuit for detecting if the test-activation voltage does not remain at the voltage detector.

32. The computer of claim 31, wherein the detector circuit comprises:

a second latch coupled to the output of the first voltage detector and to the enable circuit, the second latch maintaining power to the first voltage detector; and

a circuit coupled to the second latch for resetting the second latch.

33. The computer of claim 26 wherein the test signal comprises format bits and test code bits.

34. The computer of claim 26 wherein the enable circuit generates the enable signal for testing a flash EPROM.

35. The computer of claim 26 wherein the enable circuit Generates the enable signal for testing an SRAM.

36. The computer of claim 26 wherein the enable circuit generates the enable signal for testing an EEPROM.

37. The computer of claim 26 wherein the enable circuit generates the enable signal for testing a DRAM.

38. The computer of claim 26 wherein the enable circuit is connected to an input to the first latch.

39. The computer of claim 26 wherein the enable circuit is connected to an output of the first latch.

40. The computer of claim 26 wherein the circuit is contained within an integrated circuit package.

41. A method for generating an enable signal for testing a circuit, comprising the steps of:

detecting an activation voltage by detecting a high voltage with a first voltage detector and a second voltage detector and subsequently detecting a low voltage with the first voltage detector or the second voltage detector;

receiving a test signal;

decoding the test signal to determine if the test signal is valid; and

generating an enable signal when the activation voltage is detected if the test signal is valid.